AMENDMENTS TO THE CLAIMS

(IN FORMAT COMPLIANT WITH THE REVISED 37 CFR 1.121)

1. (CURRENTLY AMENDED) An apparatus comprising:

a logic circuit comprising (i) one or more first inputs each connected to a respective one of one or more pins, (ii) one or more second inputs each connected to a respective one of one or more bond options, (iii) one or more third inputs each connected to a respective one of one or more metal options and (iv) an output configured to present a plurality of identification codes, wherein said logic circuit is configured to generate said plurality of identification (ID) codes in response to a logical combination of (i) one or more voltage levels on said one or more first ~~inputs~~ pins, (ii) a state of said one or more bond options and (iii) a state of said one or more metal options; and

a package comprising said one or more pins, wherein said one or more pins are dedicated to providing said one or more voltage levels to respective ones of said one or more first inputs.

2. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein said ID codes comprise a silicon ID of an electronic part.

3. (CURRENTLY AMENDED) The apparatus according to claim 1, wherein said logic circuit ~~is further~~ comprises a plurality of logic gates configured to logically combine said (i) one or more voltage levels on said one or more pins connected to said one or more first inputs, (ii) a state of said one or more bond options connected to said one or more second inputs and (iii) a state of said one or more metal options connected to said one or more third inputs to generate said plurality of ID codes having a number of bits less than a total number of said metal options, said bond options, and said pins.

4. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein said one or more pins are connectable to either a voltage supply power or a voltage supply ground according to markings on said package.

5. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein each of said plurality of ID codes comprises a part number for said apparatus.

6. (PREVIOUSLY PRESENTED) The apparatus according to claim 5, wherein said part number is combined with other identification codes.

7. (PREVIOUSLY PRESENTED) The apparatus according to claim 6, wherein said other ID codes comprise one or more codes selected from the group consisting of a version number and a manufacturing number.

8. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, further comprising a register configured to capture said ID codes from said output of said logic circuit in response to an identification request.

9. (ORIGINAL) The apparatus according to claim 8, wherein said register comprises a JTAG ID code register.

10. (ORIGINAL) The apparatus according to claim 1, wherein said apparatus comprises a programmable logic device (PLD).

11. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein said metal options are set to indicate an operating voltage of said apparatus.

12. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein said bond options are set based on a style of said package of said apparatus.

13. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein said one or more pins are labeled as either a first or a second supply voltage.

14. (PREVIOUSLY PRESENTED) The apparatus according to claim 13, wherein said one or more pins are labeled as either said first or said second supply voltage based on characteristics of said apparatus.

15. (PREVIOUSLY PRESENTED) The apparatus according to claim 14, wherein said characteristics comprise one or more characteristics selected from the group consisting of volatility, price, package, metal options, operating voltage, internal structure, part category and density.

16. (PREVIOUSLY PRESENTED) A method of providing a plurality of identification codes for a single die and package combination comprising the steps of:

(A) dedicating (i) one or more pins of said package, (ii) one or more bond options and (iii) one or more metal options to generating a plurality of identification codes;

(B) generating said plurality of identification codes in response to a logical combination of (i) voltage levels on said one

or more pins, (ii) a state of said one or more bond options and (iii) a state of said one or more metal options; and

(C) providing an indication of said voltage levels to be applied to each of said one or more pins.

17. (PREVIOUSLY PRESENTED) The method according to claim 16, wherein the step (B) further comprises the steps of:

determining said voltage levels on said one or more pins;

determining said state of said one or more metal options;

determining said state of said one or more bond options; and

logically combining a result of each determining step.

18. (PREVIOUSLY PRESENTED) The method according to claim 16, further comprising the step of:

presenting a generated identification code in response to an identification request.

19. (ORIGINAL) The method according to claim 18, wherein said identification request comprises a JTAG ID code instruction.

20. (CURRENTLY AMENDED) An apparatus comprising:

means for generating a plurality of identification codes in response to a logical combination of (i) one or more voltage levels asserted at one or more pins connected to one or more first inputs, (ii) a state of one or more bond options connected to one or more second inputs and (iii) a state of one or more metal options connected to one or more third inputs; and

means for packaging said generating means comprising said one or more pins dedicated to providing said one or more voltage levels to respective ones of said one or more first inputs.

21. (CURRENTLY AMENDED) The apparatus according to claim 1, wherein said apparatus can present any more than one of said plurality of identification codes after packaging.

22. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein said apparatus changes identification code in response to a change in said one or more voltage levels applied to said one or more pins.

23. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein said package further comprises one or more pins dedicated to a test access port, at least one voltage supply pin and at least one ground pin.

24. (PREVIOUSLY PRESENTED) The method according to claim 16, further comprising:

marking voltage level indications on said package after assembly to select a particular one of said plurality of identification codes for said die and package combination.

25. (PREVIOUSLY PRESENTED) The method according to claim 16, further comprising:

changing voltage level indications provided to select different identification codes.

26. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein:

each of said one or more metal options is configured to couple said respective one of said one or more third inputs to one of a pull-up device and a pull-down device.